IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

		ATTY. DOCKET NO.: RPS920030151US1
IN RE APPLICATION OF:	§	
	§	
KENNETH DOCKSER	§	EXAMINER: **BRIAN P. JOHNSON**
	§	
SERIAL NO.: **10/699,571**	§	CONFIRMATION NO.: **1590**
	§	
FILED: ***OCTOBER 31, 2003***	§	ART UNIT: **2183**
	§	
FOR: **VECTOR EXECUTION UNIT TO PROCESS A VECTOR INSTRUCTION BY EXECUTING A FIRST OPERATION ON A FIRST SET OF OPERANDS AND A SECOND OPERATION ON A SECOND SET OF OPERANDS**	§	

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF UNDER 37 C.F.R. §41.37

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in response to a Notification of Non-Compliant Appeal Brief ("Notification") dated June 2, 2009 with respect to the Appeal Brief filed on April 29, 2009. The present Appeal Brief corrects the deficiencies noted by Examiner within the previous submission. No fees are believed to be due at this time, however, please charge any fees necessary to further the prosecution of this application to **Deposit Account Number 50-3083**.

STATUS OF CLAIMS

Claims 2-3, 5-6 and 11-20 have been canceled in the present application. Claims 1, 4, 7-10 and 21-34 remain pending and stand finally rejected by the Examiner as noted in the Final Office Action dated October 29, 2008. The rejection of Claims 1, 4, 7-10 and 21-34 is appealed.

SUMMARY OF THE CLAIMED SUBJECT MATTER

As recited by Appellants' independent Claim 1, Appellants' claimed subject matter provides: [a] microprocessor 100 (see page 1, lines 30-45; FIG. 1), comprising: a vector unit 200 (see page 1, lines 33-35; page 2, lines 5-16, 17-29, 51-60; FIG. 1; FIG. 2) to execute a vector instruction 300 (page 2, lines 47-55; page 3, lines 20-37) to perform a first operation on a first set of operands and a second operation on a second set of operands (page 3, lines 59-64); a vector register file 201 comprising a primary register file 202 and a secondary register file 204 (page 2, lines 8-11; FIG. 2) wherein the vector instruction 300 includes a first register field (306) (page 2, lines 50-55; FIG. 3) indicative of a first primary register in the primary register file 202 (page 3, lines 22-25) and a first secondary register in the secondary register file 204 (page 3, lines 23-25), a second register field (308) indicative of a second primary register in the primary register file 202 (page 2, lines 55-60) and a second secondary register in the secondary register file 204 (page 2, lines 45-50), and a third register field (310) indicative of a third primary register in the primary register file (page 2, lines 55-60) and a third secondary register in the secondary register file 204 (page 3, lines 23-25, 47-49; FIG. 2); and wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (page 3, lines 17-25), wherein the selection of the operands occurs at substantially a same time to provide an input of the three operands to the vector unit via the three inputs (page 3, lines 12-15).

Appellants' Claim 4 further provides: wherein the vector unit 200 includes a 3-input primary unit 220 and a 3-input secondary unit 230, wherein the primary unit 220 is configured to perform the first operation on the first set of operands and the 3-input secondary unit 230 is

configured to perform the second operation on the second set of operands (page 3, lines 16-24; FIG. 2).

Appellants' Claim 7 further provides: wherein the first and second operations use at least one operand from the primary register file and at least one operand from the secondary register file (page 3, lines 60-65).

Appellants' Claim 8 provides: wherein the first and second sets of operands include at least one common operand (paragraph 0029).

Appellants' Claim 9 further provides: wherein the vector register file contains information representing a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file (see paragraph 0019).

Appellants' Claim 10 provides: wherein the vector unit is configured to execute a complex computation instruction in which the imaginary portion of the first operand of the first set of operands is multiplied by an imaginary portion of a second operand in the first operation and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation (paragraph 0019).

Appellants' Claim 21 further provides: wherein the second set of operands include a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (paragraph 0026; FIG. 2).

Appellants' Claim 22 provides: wherein the first operation includes multiplying two of the three first set of operands to obtain a first product and adding or subtracting the remaining of the first set of operands to or from the first product and wherein the second operation includes multiplying two of the three second set of operands to obtain a second product and adding or subtracting the remaining of the second set of operands to or from the second product (see paragraph 0027; FIG. 4).

Appellants' Claim 22 also provides: wherein the first and second sets of operands comprise first and second sets of floating point formatted operands (paragraph 0018, 0019, 0026; FIG. 2).

Appellants' Claim 23 provides: wherein the vector instruction includes a target register field indicative of a primary target register in the primary register file and a secondary target register in the secondary register file and further wherein the vector unit is further configured to store a result of the first operation in the primary target register and to store a result of the second operation in the secondary target register (see paragraph 0028; FIG. 2).

Appellants' Claim 25 also provides: [a] vector unit to process a vector instruction 300 having an opcode 302-1, 302-2 and first, second, and third register fields (306, 308, 310) (see page 2, lines 42-52; FIG. 3) comprising: a register file including a primary register file 202 having a set of primary registers and a secondary register file 204 having a set of secondary registers, wherein each register field identifies a register in the primary register file 202 and a corresponding register in the secondary register file 204 (page 2, lines 8-19; FIG. 2); primary and secondary calculating units 220/230, wherein the primary calculating unit 220 includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands (see page 3, lines 24-36) and wherein the secondary calculating unit 230 includes first, second, and third inputs to receive, respectively, first, second, and third operands of a second set of operands (see page 3 lines 24-36; FIG. 2); and multiplexing circuitry (page 2, lines 51-59; FIG. 2) controlled by the opcode to select each of the first, second, and third operands in the first and second set of operands from the set of primary and secondary file registers identified by the register fields (see page 2, lines 60-65; page 3, lines 17-36; FIG. 2, FIG. 3).

Appellants' Claim 26 further provides: wherein the multiplexing circuitry is controlled by the opcode to select: the first operand in the first set of operands from either the first primary or the first secondary registers (paragraph 0026; FIG. 2); the second operand in the first set of operands from either the second primary or the second secondary registers (paragraph 0026; FIG. 2); and the third operand in the first set of operands from either the third primary or the third secondary registers (paragraph 0026; FIG. 2); the first operand in the second set of operands

from either the first primary or the first secondary registers (paragraph 0026; FIG. 2); the second operand in the second set of operands from either the second primary or the second secondary registers (paragraph 0026; FIG. 2); and the third operand in the second set of operands from either the third primary or the third secondary registers (paragraph 0026; FIG. 2).

Appellants' Claim 27 provides: wherein the primary calculating unit is controlled by the opcode to perform a first operation on the first set of operands and the secondary calculating unit is controlled by the opcode to perform a second operation on the second set of operands (see paragraph 0026; FIG. 2).

Appellants' Claim 28 also provides: wherein the first operation differs from the second operation (paragraph 0026; FIG. 2).

Appellants' Claim 29 provides: wherein the first and second operations both include multiplying their respective first and third operands to obtain respective first products and adding or subtracting their respective second operands to or from the respective first products (paragraph 0027; FIG. 4).

Appellants' Claim 30 further provides: wherein the first, second, and third operands of the first and second sets of operands are all floating point formatted operands (paragraph 0018, 0019, 0026; FIG. 2).

Appellants' Claim 31 provides: [a] microprocessor (100) (see page 1, lines 30-45; FIG. 1) including: an execution unit enabled to execute an asymmetric instruction, wherein the asymmetric instruction includes a set of three operand register fields (page 2, lines 47-55; page 3, lines 20-37) and a target register field and an operation code (opcode) 302-1, 302-2 (see page 2 lines 55-58; FIG. 3); a register file accessible by the execution unit and having a rank of two including a primary register file and a secondary register file (page 2, lines 8-11; FIG. 2) wherein a value in an operand register field identifies a register in the primary register file 202 and a corresponding register in the secondary register file 204 (page 3, lines 45-49); wherein the execution unit is configured to perform a first operation on a first set of three operands selected

from registers identified by the set of operand register fields (page 3, lines 16-35) and to perform a second operation on a second set of three operands also selected from the registers identified by the set of operand registers fields wherein the first and second operations and selection of the first and second sets of operands are determined by the opcode (see page 2, lines 50-60).

Appellants' Claim 32 further provides: wherein at least one condition selected from a group of conditions consisting of the first and second operations being different and the first and second sets of operands being different is true (paragraph 0017, FIG. 2).

Appellants' Claim 33 provides: wherein the execution unit is further configured to store a result of the first operation in a register of the primary register file determined by the target register field and the result of the second operation in a register of the secondary register field also determined by the target register field (see paragraph 0022, FIG. 2).

Appellants' Claim 34 further provides: including multiplexing circuitry controlled by the opcode to select a first of the first set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the first set of three operands from a second primary and a second secondary register identified by a second operand register field, a third of the first set of three operands from a third primary and a third secondary register identified by a first operand register field, a first of the second set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the second set of three operands from a second primary and a second secondary register identified by a second operand register field, and a third of the second set of three operands from a third primary and a third secondary register identified by a first operand register field (paragraph 0024; FIG. 2; FIG. 3).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. The Examiner's rejection of Claims 1, 4, 7-9 and 21-34 under 35 U.S.C. §103(a) as being anticipated by *Wang et al.* (U.S. Patent No. 5,187,796) in view of *Matsuo* (U.S. Patent No. 5,901,301) and further in view of *Sih* (U.S. Patent No. 6,557,022) is to be reviewed on Appeal.

II. The Examiner's rejection of Claim 10 under 35 U.S.C. §103(a) as being unpatentable over *Wang,* in view of *Matsuo and Sih* and further in view of *Golliver et al.* (U.S. Patent Pub. No. 2002/0004809) is to be reviewed on Appeal.

CONCLUSION

Appellants have pointed out with specificity the manifest error in the Examiner's rejections and the claim language which renders the invention patentable over the various combinations of references. Appellants, therefore, respectfully request that this case be remanded to the Examiner with instructions to issue a Notice of Allowance for all pending claims.

Respectfully submitted,

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